

Remarks

Claims 1-12 are pending, with claims 13-20 having been previously cancelled, and claims 4-7 and 12 having been withdrawn from consideration due to a restriction. Applicant renews the traversal of the restriction requirement as argued in the Response of January 9, 2008, and notes that claim 1 remains generic. By way of the present amendment, claims 8 and 9 are cancelled due to the incorporation of their subject matter into claim 1, and new claims 21-27 are added. Reconsideration and allowance of the claims is requested in light of the arguments presented below.

The following rejections are noted in the Office Action dated March 10, 2008: claims 8 and 9 stand rejected under 35 U.S.C. § 112(2) as being indefinite; claims 1, 2, 8, 10 and 11 stand rejected under 35 U.S.C. § 102(b) over Sumida (U.S. Pat. No. 5,818,282); and claims 3 and 9 stand rejected under 35 U.S.C. § 103(a) over Sumida in view of Hshieh *et al.* (U.S. Pub. 2001/0003367) and/or Hshieh *et al.* (U.S. Pub. 2001/0008788).

Applicant further notes that claims 8 and 9 are objected to for use of the term “polarity” instead of the allegedly more appropriate term “polarities.” While the cancellation of claims 8 and 9 render the objection moot, Applicant submits that the suggested amendment is unnecessary because the claims were understandable and grammatically correct as originally presented.

Applicant traverses the § 112(2) rejection of claims 8 and 9 (the subject matter of which is now incorporated into claim 1), and submits that the claim language clearly and distinctly recites the subject matter sought to be protected. A claim is not indefinite if the meaning of the claim term in question is discernable from the point of view of an ordinarily skilled artisan. *See* M.P.E.P. § 2173.02. In this case, the Examiner questions whether the claim recitation of FETs disposed in wells means that the entire FET is disposed in the well, or whether only a portion of the FET is disposed in the well. Applicant submits that the answer to such a question has no bearing on whether the recitation of a FET disposed in a well is understandable to one of skill in the art. It is well within the understanding of one of skill in the art to discern field effect transistors disposed in well structures. Moreover, the basis for the Examiner’s question appears to arise from Fig. 2a rather than from the claim language itself. Applicant submits that a

claim is not rendered indefinite merely on the allegation that a portion of the description is unclear. In Fig. 2a, the transistor 202 is shown disposed in well 206. The Examiner questions how the transistor 202 can be disposed in the well 206 when the drain 204 resides outside of the well 206. Applicant points out that the drain of transistor 202 includes the well region 206. The fact that the drain function may spill over into the region 204 does not make the residence of the transistor 202 within the well 206 any less clear.

For at least these reasons, Applicant submits that the claims are sufficiently clear and definite, and accordingly requests that the § 112(2) rejection be reconsidered and withdrawn.

Applicant traverses the § 102 rejection of claims 1, 2, 8, 10 and 11 over the Sumida reference. Applicant submits that Sumida does not disclose aspects of the claimed invention directed to a control FET disposed in a well of one polarity and a synchronous rectifier FET disposed in a well of the opposite polarity. In reference to Fig. 4, Sumida clearly discloses that MOSFET Q21 is disposed within n-drain region 25 and that MOSFET Q22 is disposed within n-drain region 31. Moreover, and with respect to claim 10, Applicant submits that Sumida does not disclose aspects of the claimed invention directed to the integrated circuit having no isolation region between the control FET and the synchronous rectifier FET. The Sumida reference clearly teaches an isolation region 27a disposed between MOSFETS Q21 and Q22.

For at least these reasons, the Sumida reference does not teach all the features recited in Applicant's claims. As such, Applicant submits that the § 102 rejection of claims 1, 2, 8, 10 and 11 is improper, and requests that it be reconsidered and withdrawn.

Applicant traverses the § 103 rejection of claims 3 and 9 over the Sumida reference in view of the Hshieh '367 reference and/or the Hshieh '788 reference. Applicant submits that the Hshieh references appear to teach or suggest nothing to cure the underlying deficiencies of the Sumida reference as noted above. The Hshieh references are relied upon for allegedly disclosing trench-type FETs, which are not expressly disclosed by Sumida, and appear to disclose nothing regarding the respective wells of a control FET and a synchronous rectifier FET being opposite in polarity.

For at least these reasons, the proposed combination of Sumida with Hshieh '367 and/or the Hshieh '788 is improper for failing to teach or suggest all the features recited in Applicant's claims. As such, Applicant submits that the § 103 rejection is improper, and requests that it be reconsidered and withdrawn.

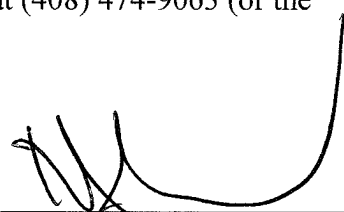
Applicant further submits that the art of record does not teach the subject matter additionally recited in new claims 21-27. For example, claims 21 and 22 respectively include one or more additional FETs to control gate switching of the recited control FET and synchronous rectifier FET, and an inductor of the down converter to which a source contact of the control FET and a drain contact of the synchronous rectifier FET are connected. Claims 23 and 24 respectively recite low-ohmic connections of the source contact of the control FET and the drain contact of the synchronous rectifier FET to mitigate resistive and inductive parasitics of the integrated circuit, and that the integrated circuit has a parasitic inductance on the order of 1 nH or less. Claims 25 and 26 respectively recite that the down converter includes a voltage input connected to the drain contact of the control FET and the source contact of the control FET connected to the drain contact of the synchronous rectifier FET via a conductive plug in the substrate. Claim 27 recites that the control FET includes a gate driven by a control block supplied by an external capacitor.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Applicant further requests an indication of allowance for dependent claims 4-7 along with an indication of allowance of generic claim 1. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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